Description

SYSTEM FOR SYNCHRONOUS SAMPLING AND TIME-OF-DAY CLOCKING USING AN ENCODED TIME SIGNAL

Technical Field

This invention relates generally to electronic instruments which sample analog input signals to produce corresponding digital signals, and more specifically concerns synchronization of the sampling function in a plurality of such instruments.

Background of the Invention

Various electronic instruments, including, for example, protective relays for power systems and electricity meters, sample analog input signals by means of an analog-to-digital converter to produce digital signals which are then processed to produce specific information from the input signals which relates to the function of the instrument. Appropriate action is taken, relative to the instrument, as needed, in response to that information. For instance, in a protective relay, if the information from the input signals indicates a fault on the power line, the instrument may trip the current breaker for that portion of the line.

In certain situations/system arrangements, it is important that sampling of the analog input signals be made simultaneously by multiple instruments, again for instance, simultaneous sampling of line voltage and current input signals in a plurality of protective relays.. This presents a challenge when the instruments are not all located in close physical proximity. A number of solutions concerning the synchronous sampling of inputs to multiple electronic instruments, however, are known. One such system uses a repeating time pulse, derived from the Global Positioning System.

Many of the electronic instruments which utilize sampling functions also have a time-of-day clock and calendar which the instrument uses to time-tag particular reports or other information which the instrument generates. One example

of such a report is an oscillograph report from a power system protective relay; another example is a revenue report from an electricity meter. It is important that the time-of-day clocks in the multiple devices are synchronized to all report the same time, at the same instant, on time. Many current devices use an encoded time-of-day signal, such as an IRIG-B signal, to synchronize their time-of-day internal clocks.

As presently configured, most such instruments use two control signals to accomplish desired synchronization, one control source being a periodic pulse by which each device synchronizes its sampling of input signals to be measured, and the other being a nonperiodic encoded time-of-day signal to which the device synchronizes its time-of-day clock.

While the use of two separate control signals has proved to be workable, it is desirable to have a single control signal to synchronize both data sampling (or other periodic action) and the time-of-day clock in electronic instruments.

Summary of the Invention

Accordingly, the present invention is a system for synchronous sampling of analog signal inputs for a plurality of electronic instruments, using an encoded time signal, comprising: an externally generated encoded time signal provided to the plurality of electronic instruments suitable for insuring accurate time-of-day clock synchronization for the electronic instruments; an edge detector responsive to the encoded time signal to produce a series of pulses based on the edges of the encoded time signal; and a phrase-locked loop assembly producing an output sampling synchronization signal which is phrase-locked to said pulses at the output of the edge detector, such that the output sampling synchronization signal occurs at the beginning of each predetermined time period with successive synchronization signals being evenly spaced in the interval between the beginning of each successive predetermined time, for synchronization of data sampling in said plurality of instruments.

Brief Description of the Drawings

Figures 1A-1C show the encoding of an IRIG-B time signal.

Figure 2 is a diagram showing a complete IRIG-B signal frame representing one second of time of day.

Figure 3 is a block diagram showing the system of the present invention using an encoded time signal to produce a sampling synchronization signal.

Figure 4 is a block diagram which is an alternative to the system of Figure 3.

Best Mode for Carrying Out the Invention

In the present invention, an encoded time-of-day signal, such as an IRIG-B signal, which is currently used to synchronize the time-of-day clocks in a plurality of electronic instruments, is also used to produce sampling synchronization signals for the same plurality of instruments, instead of having two separate synchronization signals, one for sampling and the other for time of day. Although the embodiment described concerns sampling signals, it should be understood that the encoded time of day signal could be used for synchronization of other instrument operations, including for instance synchronization of various test procedures and communication procedures, among others.

In the described embodiment of the present system, the encoded time-of-day signal is an IRIG-B (U.S. Army IRIG standard 200-89). However, it should be understood that the present invention is not limited to an IRIG-B signal; rather, any encoded time signal which can be used to synchronize time clocks in a plurality of electronic instruments can be used to produce a synchronous data sampling signal as well.

A conventional IRIG-B time signal, using pulse width modulation to encode information concerning the time of day is shown in Figures 1A-1C. In a 10-millisecond bit, a binary coded digit is encoded as a zero (pulse width of 2 milliseconds) shown at 12 or a one (pulse width of 5 milliseconds) shown at 14. Each IRIG-B complete frame (a single frame is shown in Figure 2) represents one second in time. Separate frames are provided for

each successive second. Each IRIG-B frame is separated by two successive "P" bits from the next successive frame, each "P" bit having an 8-millisecond pulse (shown at 16) out of the 10-millisecond bit.

Figure 2 shows how the IRIG signal is transmitted, as a series of ones and zeros as set forth above, providing an indication of seconds, minutes, hours, days (0-99) and hundreds of days (0-3). The IRIG-B information is transmitted simultaneously to a plurality of instruments (e.g. a plurality of protective relays for a power system) operating in synchronization. The IRIG-B signal sets the time-of-day clock in each of the devices so that the time of day is the same in each of the plurality of devices in a particular system.

In Figure 2, the complete IRIG-B transmission identifying one particular second in a year is shown at 17. The encoding for seconds is designated at 18, minutes at 22, hours at 26, 0-99 days at 30, and hundreds of days at 32. The particular second identified is the 35th second, of the 12th minute, of the 17th hour, of the 209th day. An "R" field 34, comprising two successive "P" bits, separates successive frames. In the present invention, the IRIG-B encoded time signal or other encoded time signal is also used for its conventional time-of-day clock synchronization of a plurality of devices. However, it is also used to produce a data sampling (or other function) synchronization signal for the same devices.

Referring to Figure 3, the IRIG-B time-encoded signal is first applied to a conventional edge detector 40. The edge detector 40 will produce a pulse whenever an edge (rising or falling) of the IRIG-B signal is detected.

Referring again to Figure 1, the time between successive edges of the IRIG-B signal could be 2, 5 or 8 milliseconds, based on a 10-millisecond bit. Thus, the output of the edge detector 40 will be a series of pulses, separated by 2, 5 or 8 milliseconds. Each edge will be a multiple of 1kHz away from the last edge. The output of the edge detector 40 is applied to a phase-locked-loop 42 which is arranged to produce an output signal of selected frequency, 8kHz in the embodiment shown, phase-locked to the pulses from the edge detector. Since

the transitions of the output signal from the phase-locked-loop occur simultaneously with transitions in the IRIG-B signal input, a data sampling synchronization signal occurs precisely at the beginning of each second, as defined by the IRIG-B input signal, in particular, the rising edge of the second "P" bit in the "R" field 32. The 8kHz output signal on line 47 is the data sampling synchronization signal for the plurality of synchronized devices.

The phase-locked-loop 42 includes a phase detector 43 which is responsive to the output of the edge detector 40 and a feedback circuit from the output of the phase-locked-loop to determine whether there is any phase difference between the two signals. If there is no phase difference, then the two signals are exactly in phase, and the output of the phase detector is zero. If there is a difference, then the output of the phase detector is some number representative of the phase difference. This output is supplied to a filter 44, the purpose of which is to reduce jitter in the signal from the phase detector. In the embodiment shown, this is a divide by 32 circuit. For example, if a count of 100 is provided at the input to the filter 44, a count of three is provided at the output.

The output of the filter controls a numerically controlled counter (NCO) 46, which is designed to produce an output signal (line 47) of selected frequency, *i.e.* 8kHz in this particular embodiment. It could, however, be other integral multiples of 1kHz, including 1kHz, 2kHz, 3kHz, etc. The NCO in operation counts nominally to the output frequency, which in the embodiment shown is 8kHz. The count is adjusted by the output of the filter (+/-); the adjustment allows the system to lock to the incoming signal. The output of counter 46 is applied to the feedback circuit 50 for the phase-locked-loop. The feedback circuit 50 converts the 8kHz signal to a 1kHz signal, which is then applied to the phase detector 42 for comparison with the signal from the edge detector.

Figure 4 shows another embodiment, in a simplified form, in which edge detector 60 responds only to the positive (rising) edges of the IRIG-B encoded time signal input, meaning

a pulse every 10 milliseconds, *i.e.* a 100Hz signal. The phase-locked-loop 62 in Figure 4 is designed to lock to a periodic 100Hz input signal and produce an output data sampling synchronization signal. As long as the phase-locked-loop 62 is designed to produce an output signal with a frequency of an integral multiple of 100Hz, the output will be data sampling synchronization signals precisely at the beginning of each second and evenly spaced between each successive second at a selected frequency which is a multiple of 100Hz, *i.e.* 100Hz, 200Hz, 300Hz, etc.

Thus, a single control signal to a plurality of devices to be synchronized in operation will result in both time-of-day clock synchronization and data sampling synchronization for the plurality of instruments. Again, while in the embodiment shown an IRIG-B encoded time-of-day signal is used, other nonperiodic encoded time signals can be used for synchronization of the data sampling system, *i.e.* the invention is not limited an IRIG-B signal. Further, the invention is not limited to data acquisition, i.e. data sampling. It could be used for other synchronization functions as well.

It should also be understood that the IRIG-B time signal or other time signal, provided to a single relay or similar device, such as a meter, could be used to provide very accurate sampling signals for that device in addition to providing time-of-day information for reports, etc. In such an arrangement, the relay includes a phase-locked loop which provides an output signal at a specific selected frequency, *e.g.* 8kHz. In operation, the data acquisition system for the relay or meter will be phase-locked to the IRIG-B or other time source. If there is no IRIG-B signal available, or if high accuracy is not required (an example of high accuracy requirements is when synchophasors are used in the device), then the internal sampling system in the equipment can be used.

Although a preferred embodiment of the invention has been disclosed for purposes of illustration, it should be understood that various changes modifications and substitutions can be incorporated in the embodiment without departing from the

spirit of the invention which is defined by the claims which follow.

What is claimed is: